|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Function** | **Type** | **Input** | **Outputs** | | | | | | | | | | |
| **OpCode** | **A1A0** | **Add/Sub** | **Cin** | Reg WR | Mrd | mwr | **RegDst (SW)** | **MemtoReg (LW)** | **ALUSrc (IMM)** | **Branch** | **Jump** |
| AND | R | 0000 | 00 | X | X | 1 | X | X | 1 | 1 | 0 | 0 | 1 |
| OR | R | 0001 | 01 | X | X | 1 | X | X | 1 | 1 | 0 | 0 | 1 |
| ADD | R | 0010 | 10 | 0 | 0 | 1 | X | X | 1 | 1 | 0 | 0 | 1 |
| SUB | R | 0011 | 10 | 1 | 1 | 1 | X | X | 1 | 1 | 0 | 0 | 1 |
| ANDi | I | 0100 | 00 | X | X | 1 | X | X | 0 | 1 | 1 | 0 | 1 |
| ORi | I | 0101 | 01 | X | X | 1 | X | X | 0 | 1 | 1 | 0 | 1 |
| ADDi | I | 0110 | 10 | 0 | 0 | 1 | X | X | 0 | 1 | 1 | 0 | 1 |
| SUBi | I | 0111 | 10 | 1 | 1 | 1 | X | X | 0 | 1 | 1 | 0 | 1 |
| SLT | R | 1000 | 11 | 1 | 1 | 1 | X | X | 1 | 1 | 0 | 0 | 1 |
| SLTi | I | 1001 | 11 | 1 | 1 | 1 | X | X | 0 | 1 | 1 | 0 | 1 |
| BEQ | I | 1010 | 10 | 1 | 1 | 0 | X | X | X | X | 0 | 1 | 1 |
| BNE | I | 1011 | 10 | 1 | 1 | 0 | X | X | X | X | 0 | 1 | 1 |
| J | J | 1100 | XX | X | X | 0 | X | X | X | X | X | X | 0 |
| Unused | -- | 1101 | XX | X | X |  |  |  |  |  |  |  |  |
| LW | I | 1110 | 10 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| SW | I | 1111 | 10 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |